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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,645	03/29/2004	Ming-Dou Ker	06720.0118-00	9584
570	7590	05/19/2005	EXAMINER	
AKIN GUMP STRAUSS HAUER & FELD L.L.P. ONE COMMERCE SQUARE 2005 MARKET STREET, SUITE 2200 PHILADELPHIA, PA 19103			NATALINI, JEFF WILLIAM	
			ART UNIT	PAPER NUMBER
			2858	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/810,645

Applicant(s)

KER ET AL.

Examiner

Jeff Natalini

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 March 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

Information Disclosure Statement

1. The listing of references in the specification ("Transmission Line Pulsing Techniques for Circuit Monitoring" by Intel Corp- pg 7-8 para 25 in the specification) is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because figures 1-3 contain handwritten items, that makes it hard to read. Also figures 1a and 1b contain boxes that need to be specifically labeled and not just numbered so they are easily identifiable. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the (claims 5 and 15) where the pulse generator includes a biasing source; (claims 6-9 and 23-27) where a

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specific semiconductor device is specifically hooked up to the system; (claim 12) no second pulse generator is shown providing a second ESD pulse; must be shown or the feature(s) canceled from the claim(s). A separate figure should be shown for the testing of a MOS, SCR/LVTSCR, and FOD/BJT as they are described differently in the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claim 31 is objected to because of the following informalities:

- It is stated in that “at least one ESD-scale pulses” is generated, but in the claim, two pulses are specifically generated (first and second ESD scale pulse), therefore it should state “at least two ESD-scale pulses are generated” and this should be changed throughout. Also there is no antecedent basis for “the multi-terminal semiconductor device”, this should be corrected by at adding “semiconductor” between multi-terminal and device on the first indented line in the claim, so to read “providing a multi-terminal semiconductor device”

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-6, 10, 12-15, 17-23, 28-29, 31, 32, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by (Chen et al. “Investigation of the Gate-Driven Effect and Substrate-Triggered Effect on ESD Robustness of CMOS Devices” herein to be referred to as Chen).

In regard to claims 1, 5, 12, 15, 18, 21, and 31, Chen discloses a system for measuring electrostatic discharge (ESD) characteristics of a semiconductor/multi-terminal device (abstract), comprising: at least one pulse generator generating ESD-

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scale pulses (fig 5a, 8a, 13, or 14)); a first point of the semiconductor device (TLPG- seen as an input into the drain in figs (5a, 8a, 13, or 14)) receiving a first ESD-scale pulse from the at least one pulse generator, a second point of the semiconductor device receiving the first ESD-scale pulse from the at least one pulse generator (pg 191, fig 4 shows different points of the drain being connected) at least a third point of the semiconductor device receiving a second ESD-scale pulse from a second pulse generator (pg 197 figs 13 and 14 show a biasing source generating a pulse into the gate); and a data collector to collect data on the ESD characteristics of the semiconductor device (abstract states that data is collected and measured and figures on pg 193-195 show that the device was hooked up to display and analyze data); detecting if a leakage current flows in the semiconductor device (pg 194 column 1 continued to col 2; measured leakage currents are shown in fig 8b)).

In regard to claims 2, 17, 22, and 32, Chen discloses wherein the semiconductor device is a MOS transistor (fig 4).

In regard to claims 3, 4, 13, 14, 19, 20, and 35, Chen discloses wherein a transmission line pulse generator is able to generate ESD pulses (abstract; also different pulses are generated in fig 5a pg 192 or 21a pg 202, which allows two different pulses to be TLP driven).

In regard to claim 6 and 23, wherein the MOS transistor includes a source and drain to receive the first ESD pulse (fig 11 pg 196, the ESD pulse is applied to the drain in different positions as seen in fig 4, the source also receives the signal as they are tied

together and is seen in the side graphs) and a gate to receive the second ESD pulse (this is seen in figs 12-14 pg 197).

In regard to claims 10 and 29, Chen discloses a detector to detect a leakage current in the device (pg 194 column 1 continued to col 2; measured leakage currents are shown in fig 8b).

In regard to claim 28, Chen discloses a data collector to collect data regarding the ESD characteristics of the semiconductor device (abstract states that data is collected and measured and figures on pg 193-195 show that the device was hooked up to display and analyze data).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 9, 26, 27, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen.

In regard to claims 9, 26, and 27, Chen teaches all that is disclosed above to reject claim 6.

Chen lacks specifically disclosing where in both a FOD and BJT the emitter and collector receive the first ESD pulse, and a base receives the second ESD pulse.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to use engineering intuition knowing that MOSFETS and BJTs/FOTs are similar devices even though are separated by analog and digital realms, the source and drain/similar of a MOS are similar to collector/emitter of FOT/BJT and gate of MOS is similar to the base of FOT/BJT and test the structure accordingly even though it is digital in order to determine proper electrostatic properties of semiconductor devices.

In regard to claim 33, Chen lacks specifically where the second pulse is supplied to the third terminal before the first pulse is applied to the second and third.

MPEP 21144.04 *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) says that selection of any order of performing process steps is prima facie obvious in the absence of new and unexpected results.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chen to apply the second pulse before the first pulse in order to perform variations of tests so to be able to provide the best analysis on electrostatic properties on semiconductor devices.

9. Claims 7, 8, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Ker et al. (US 5576557).

Chen lacks wherein an SCR and LVTSCR includes an anode and a cathode to receive the first ESD pulses, and a substrate to receive a second ESD pulse.

Ker et al. teaches SCR and LVTSCR includes an anode and a cathode to receive an ESD pulse, and a substrate to receive a second ESD pulse.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chen to include testing a SCR and LVTSCR with an anode and cathode to receive an ESD pulse, and a substrate to receive a second ESD pulse as disclosed by Ker et al. in order to be able to provide proper protection to CMOS ICs (col 1 line 11-15).

10. Claims 11, 16, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Consiglio (US 5519327).

Chen lacks wherein there is a switching device coupled to the pulse generator(s) and the detector to switch a connection between the pulse generator(s) and the detector.

Consiglio teaches having a switch coupled between a pulse generator and the detector to detect the leakage current so to switch the connection between the pulse generator and the detector (fig 3, chart; abstract).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chen to include a switch coupled between a pulse generator and the detector to detect the leakage current as taught by Consiglio in order to determine the leakage current after each pulse is applied to the DUT (abstract).

11. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Barth et al. ("TLP Calibration, Correlation, Standards, and New Techniques" herein to be referred to as Barth).

Chen lacks specifically stating wherein a step of detecting whether leakage current flows in the multi-terminal device before providing the first and second ESD-scale pulse.

Barth et al. teaches that the concept of measuring leakage current in TLP test systems is for the user to know how the leakage current evolved as the pulse test current amplitude was increased.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Chen to detect whether a leakage current flows before providing the pulses to the device in order to know how the leakage current evolved as the test pulses were increased as taught by Barth et al.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Allard, Jr. et al. (US 6541981) teaches transmission line pulse testing of electrostatic discharge devices, contains a pulse generator to transmit pulses to a DUT. Fukuda (US 4823088) teaching testing semiconductor devices for electrostatic damage, applies three different signals to three different places on the device on test. Consiglio (US 5675260) teaching a single signal generator that is able

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to connect to multiple places, four places for a transistor through contact pads having controllable pulsing means.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on 571-272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff Natalini




ANJAN DEB
PRIMARY EXAMINER